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	Application No.	Applicant(s)
Notice of Allowability	10/572,185	SAWADA, TOSHIAKI
	Examiner	Art Unit
	Vincent Q. Nguyen	2858
The MAILING DATE of this communication appeall claims being allowable, PROSECUTION ON THE MERITS IS therewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIP	(OR REMAINS) CLOSED in this applied or other appropriate communication IGHTS. This application is subject to	plication. If not included will be mailed in due course. THIS
1. This communication is responsive to 6/27/2007.		
2. The allowed claim(s) is/are <u>1-13</u> .		
 Acknowledgment is made of a claim for foreign priority ur a) ⊠ All b) □ Some* c) □ None of the: 1. ⊠ Certified copies of the priority documents have 2. □ Certified copies of the priority documents have 	e been received.	· •
3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		
4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.		
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted. (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached 1) ☐ hereto or 2) ☐ to Paper No./Mail Date 		
(b) including changes required by the attached Examiner's Paper No./Mail Date	s Amendment / Comment or in the C	Office action of
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in the	.84(c)) should be written on the drawir he header according to 37 CFR 1.121(c	ngs in the front (not the back) of d).
5. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.		
Attachment(s) I. ☑ Notice of References Cited (PTO-892)	5. ☐ Notice of Informal P	atent Application
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summary	(PTO-413),
B. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>5/14/2007</u>	Paper No./Mail Dat 7. ☐ Examiner's Amendn	
I. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. ⊠ Examiner's Stateme	nt of Reasons for Allowance
	V. hg	yer.
	VINCEN PRIMAR	T Q. NGUYEN IY EXAMINER

Art Unit: 2858

DETAILED ACTION

This Office action is in response to Applicant's Amendment filed 6/27/2007.

Allowable Subject Matter

- 1. Claims 1-13 are allowed.
- 2. The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or suggest a semiconductor switch circuit having first semiconductor switch, second semiconductor switch, and third semiconductor switch are operated and controlled in the OFF state by the switch control means, said first and second voltage application means are each controlled to the ON state, the first voltage application means applies the potential of the input terminal to a first voltage application point that is the junction between said first semiconductor switch and second semiconductor switch, and the second voltage application means applies the potential of the output terminal to a second voltage application point that is the junction between said second semiconductor switch and third semiconductor switch, as recited in dependent claim 1;

a semiconductor switch circuit having two semiconductor switches are operated and controlled in the OFF state by the switch control means, said voltage application means is controlled to the ON state, and applies to a voltage application point that is the junction of said two semiconductor switches the potential of the input terminal or output terminal to which said one of the semiconductor switches that is connected in parallel to the voltage application means is connected, as recited in the independent claim 2 and in combination of the claims.

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Any comments considered necessary by applicant must be submitted no later

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than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance."

Contact Information

3. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Vincent Q. Nguyen whose telephone number is (571)

272-2234. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Andrew Hirshfeld can be reached on (571) 272-2168. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

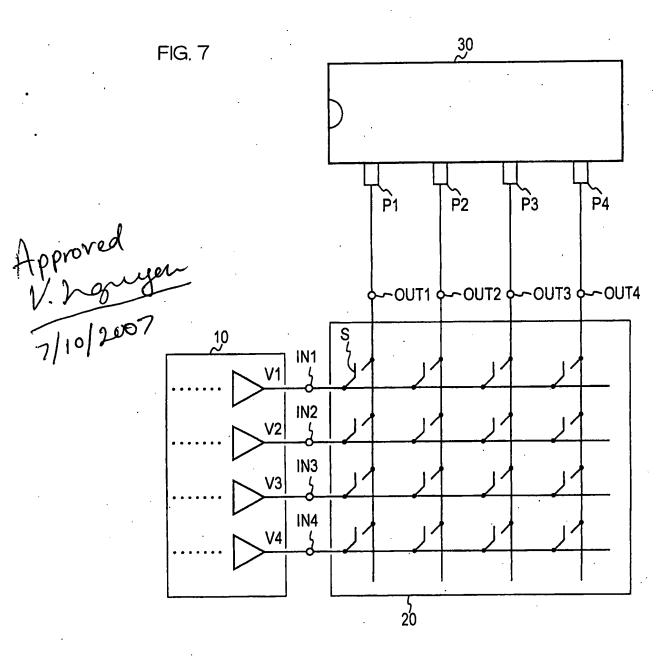
Vincent Q. Nguyen

V. Ingryon

JUN 2 7 2007

Replacement Sheet 2 of 2
"Semiconductor Switch Circuit"
Inventor: Toshiaki Sawada

S/N: 10/572,185 Contact: Gallagher & Lathrop (415) 989-8080 Docket: NAA236



PRIOR ART

Replacement Sheet 1 of 2
"Semiconductor Switch Circuit"
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S/N: 10/572,185
Contact: Gallagher & Lathrop (415) 989-8080
Docket: NAA236

FIG. 8 A

PRIOR ART

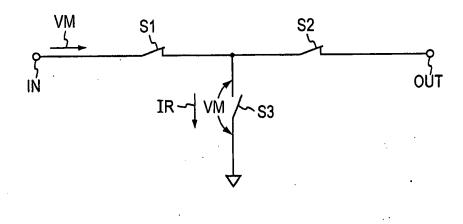


FIG. 8 B

PRIOR ART

